CS-02-084

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December 12, 2003

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

| Serial No. 10/662,673 09/15/03 |

Indrajit Manna et al.

ELECTROSTATIC DISCHARGE PROTECTION DEVICE WITH COMPLEMENTARY DUAL DRAIN IMPLANT

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

- U.S. Patent 6,521,946 to Mosher, "Electrostatic Discharge Resistant Extended Drain Metal Oxide Semiconductor Transistor," describes a doped region under a drain for ESD protection.
- U.S. Patent 6,365,932 to Kouno et al., "Power MOS Transistor," discloses a p-type base region in an N-well partly overlapping a deep N+ region.
- U.S. Patent 5,543,650 to Au et al., "Electrostatic Discharge Protection Circuit Employing a MOSFET Device," discloses an n-well with P+ implants for ESD protection.

Sincerely,

Stephen B. Ackerman,

Req. No. 37761

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citation if not in conformance and not considered. Include copy of this form with next communication to the applicant